POUGHKEEPSIE, NEW YORK

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The IAS Computer

Today I visited the IAS computer laboratory as the guest of Mr. W. Ware. A large scale digital computer is under construction there, and one of the important uses to which it will be put is the study of meteorology.

It calculates in the binary system with 40-digit numbers (which are equivalent to 12-digit decimal numbers). The basic speed for simple operations will be about 10 microseconds while multiplications will average about 300 microseconds.

The storage will be either with Selectrons or with Williams' type of cathode ray tube operation. There will be one or more storage tubes per binary column in the computer.

At the moment, Selectrons look as if they are going to be able to store only 256 bits of information. RCA still thinks they are just around the corner.

When complete, the computer itself will be about 3 feet high, 12 feet long, and 2 feet wide. In addition, there will be the input and output equipment and power supplies.

In order to introduce instructions and data to the computer, the information is first punched on teletype type with a modified teletype punch. A second teletype punch is used to punch a second tape while the punching is verified against the first tape.

The paper tape is then put into a magnetic recorder which transfers the information to a wire.

The wire is then fed into a reader at 100KC whence the information proceeds to the computer electrically.

A similar process in reverse is used to print the results of a calculation.

I presume that the teletype apparatus has been modified to use binary digits since the translation from binary coded decimal to pure binary

is easier than the translation from standard teletype symbols to binary. In any event, all of the translation is done in the computer so that the operators use only decimal numbers.

Two instructions are included in each word and I believe that 8 bits are used to specify the operation to be performed and 12 bits are used for the address. In this case, the upper limit of storage is 4096 words of 40 binary digits. It seems unlikely that they will use as much storage as this unless some much superior means of storage appears.

The present stage of development is that the input output apparatus is in working order and the arithmetic circuits are nearly done. As yet, they have no storage and appear to have done little more than the paper work on the main control although I believe that they have nearly completed the arithmetic controls (for the individual operations such as multiply, divide, add, subtract, etc.).

Work is proceeding on the Williams' tube in order to have a way out in case the Selectron is not completed soon enough.

The drive for the magnetic wire is by means of two synchro motors. One is used as a 3-phase 400 cycle induction motor to drive both spools. Via a mechanical differential the second synchro motor is employed in a servo circuit to rotate one spool with respect to the other to compensate for the difference in diameter when one spool contains more wire than the other. Reading is done during acceleration and no strenuous efforts have been exerted to achieve fast starts and stops.

It is intended that the magnetic wire will ultimately be under the control of the computer, but no attempt will be made to set this up until the computer is in operation with manual wire control.
The arithmetic circuits consist of three double registers (two sets of 40 triggers in each), an adding circuit, and controls.

The switches are connected to triggers as shown in Fig. 1. The switch is controlled by a voltage applied to grid a. if grid a is positive, the left hand triode of the two in the switch always conducts and the right

hand one never can, so no signal can reach the trigger. Only if grid a is negative and grid b is positive can a signal reach the trigger and in this case the trigger is turned on (right side conducting). Enough of these switches are connected to each trigger for the operations about to be described. I was told that one triode of the type on the left of the switch is used for every five of the type on the right. In order for this to be possible, it seems to me that there must be another resistor in the cathode circuit of the right hand triodes.

A small section of one of the three identical registers is shown in Fig. 2. Each square represents a trigger and some switches. Either the top or the bottom triggers can be cleared, and the numbers can all be moved simultaneously from top to bottom shifting left, or from top to bottom shifting right, or from bottom to top.

It is also possible to read to and from the top*and bottom sections to other parts of the computer.

The arrangement of these three registers in the arithmetic circuits is shown in Fig. 3, which illustrates the process of addition. One addend is in the lower section of the accumulator while the other addend is located in the multiplicand register. The adding circuits and the digit sensing combine to make an adder which includes a complete carry with every addition. The type of carry is not entirely clear to me, but it seems to lie somewhere between a simultaneous carry and the consecutive type of carry used in the 604. The carry ripples down very fast (10 microseconds) even if all 40 triggers contained 1's and generate carries. This speed is to be compared with a 1 microsecond period which is used for shifts which do not involve carries.

The multiplication circuit is shown in Fig. 4. The "accumulator" of Fig. 4 includes the "accumulator register", "adding circuits" and "digit sensing" of Fig. 3.

Initially, the multiplier is in the multiplier register and the multiplicand is in the multiplicand register (where it remains for the duration of the multiplication) while the accumulator is empty. The least significant digit is on the right while the most significant digit is on the left.

The rightmost digit (least significant digit) of the multiplier is sensed and if it is a 1 the multiplicand is added to the accumulator and the 1 is replaced with a zero. If it is a zero, the accumulator and the multiplier register are both shifted left one digit: the rightmost digit in the accumulator is shifted into the leftmost column of the multiplier register which becomes available as the multiplier moves right.

Then the rightmost digit is sensed again and the process is repeated, until 40 shifts have been made and this is the signal that multiplication is complete.

The final result of multiplication is that the multiplicand still stands in the multiplicand register, the more significant half of the product stands in the accumulator; the less significant half of the product stands in the multiplier register; and the multiplier has been lost.

If double-length multiplication is being done, both halves of the product may be saved, but if not, the product is rounded off and the contents of the multiplier are discarded. This whole process requires an average time of about 300 microseconds.

Division is carried out by putting the divisor in the multiplicand register, the dividend in the accumulator, and developing the quotient in the multiplier register. Division takes the same length of time as the longest multiplications (500 microseconds).

N. Rochester

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